WHAT IS CLAIMED IS:

1. A data processing device reading in and executing instructions in a certain sequence, the data processing device comprising:

a fetch portion for reading in a computational instruction;

a decoding portion for decoding the computational instruction that has been read in;

an execution portion for executing the decoded computational instruction; and

an instruction overriding control circuit that overrides, of one or a plurality of subsequent instructions that follow the computational instruction in said sequence and are associated with the computational instruction, all but one of the subsequent instructions, in accordance with an execution result of the computational instruction.

2. The data processing device according to Claim 1, wherein said one or plurality of subsequent instructions is a subsequent instruction group including a plurality of instruction strings.

3. A program conversion device for reading in a descriptive program and converting it into a machine language program, the program conversion device comprising:

an instruction detection portion for detecting from instruction strings of the descriptive program an instruction involving a condition or decision; and

an instruction rewriting portion for rewriting a condition/decision instruction detected by the instruction detection portion into instruction strings including a computational instruction and one or a plurality of subsequent instructions following the computational instruction and associated with the computational instruction.

4. The program conversion device according to Claim 3, wherein said one or plurality of subsequent instructions is a subsequent instruction group including a plurality of instruction strings.

5. A data processing device reading in and executing instructions in a certain sequence, the data processing device comprising an instruction

Claims 3-4, 7-8, 11-12, & 15-16 accepted for 717/140 as an assembler by T. Ingberg & T. Dam on 5/10/04

memory, a fetch portion, a decoding portion, an instruction execution portion, and an instruction overriding control portion,

wherein the instruction memory stores a first subsequent instruction corresponding to a first conditional instruction from which the first condition has been eliminated, a second subsequent instruction corresponding to a second conditional instruction from which the second condition has been eliminated, and a command instruction that is arranged prior to the first subsequent instruction and the second subsequent instruction in the instruction sequence, and that indicates that the first subsequent instruction and the second subsequent instruction have contradictory execution conditions, and that indicates the contradictory execution conditions generated from the first condition and the second condition;

wherein the fetch portion fetches the command instruction from the instruction memory;

wherein the decoding portion decodes the fetched command instruction;

wherein the instruction execution portion executes the decoded command instruction; and

wherein the instruction overriding control portion checks the execution result of the instruction command to determine which of the first condition and the second condition is satisfied, and overrides the instruction of the first subsequent instruction and the second subsequent instruction for which the condition is not satisfied.

6. The data processing device according to Claim 5, wherein the first conditional instruction, the second conditional instruction, the first subsequent instruction and the second subsequent instruction each consist of one instruction or an instruction group including a plurality of instruction strings.

7. A program conversion device for reading in a descriptive program and converting it into a machine language program, the program conversion device comprising:

a first instruction detection portion for detecting from instruction strings of the descriptive program an instruction for which there is a possibility that a state of a processor is updated;

a second instruction detection portion for detecting from the entered instruction strings a conditional instruction that is executed depending on a state of the processor;

a first judgment portion for judging whether a first conditional instruction and a second conditional instruction that have been detected by the second instruction detection portion are arranged successively after an instruction detected by the first instruction detection portion;

a second judgment portion for judging whether the execution conditions of the first conditional instruction and the second conditional instruction contradict one another.

a command instruction retrieval portion for retrieving from the machine language instruction code a command instruction, which indicates the same process execution as the instruction detected by the first instruction detection portion, and which indicates that the subsequent first conditional instruction and second conditional instruction are executed at contradictory conditions;

an instruction rewriting portion for rewriting an instruction string detected by the first instruction detection portion and the second instruction detection portion into a first subsequent instruction corresponding to the first conditional instruction from which the first condition has been eliminated, a second subsequent instruction corresponding to the second conditional instruction from which the second condition has been eliminated, and the command instruction.

8. The program conversion device according to Claim 7, wherein the first conditional instruction, the second conditional instruction, the first subsequent instruction and the second subsequent instruction each consist of one instruction or an instruction group including a plurality of instruction strings.

9. A data processing device reading in and executing instructions in a certain sequence, the data processing device comprising:

a fetch portion for reading in a computational instruction;

a decoding portion for decoding the computational instruction that has been read in;

an execution portion for executing the decoded computational instruction; and

an instruction overriding control circuit which decides, in accordance with an execution result of the computational instruction, whether to override a subsequent instruction that follows the computational instruction in said sequence and is associated with the computational instruction, and which overrides this subsequent instruction in accordance with that decision.

10. The data processing device according to Claim 9, wherein said subsequent instruction is a subsequent instruction group including a plurality of instruction strings.

11. A program conversion device for reading in a descriptive program and converting it into a machine language program, the program conversion device comprising:

an instruction detection portion for detecting from instruction strings of the descriptive program an instruction involving a condition or decision;

an instruction rewriting portion for rewriting a condition/decision instruction detected by the instruction detection portion into instruction strings including a computational instruction and a subsequent instruction following the computational instruction and associated with the computational instruction.

12. The program conversion device according to Claim 11, wherein said subsequent instruction is a subsequent instruction group including a plurality of instruction strings.

13. A data processing device reading in and executing instructions in a certain sequence, the data processing device comprising an instruction memory, a fetch portion, a decoding portion, an instruction execution portion, and an instruction overriding control portion,

wherein the instruction memory stores a subsequent instruction corresponding to a conditional instruction from which the condition has been eliminated, and a subsequent execution condition command instruction that is arranged prior to the subsequent instruction in the instruction sequence, and that indicates that the subsequent instruction has an execution condition, and that indicates that execution condition;

wherein the fetch portion fetches the subsequent execution condition command instruction from the instruction memory;

wherein the decoding portion decodes the fetched subsequent execution condition command instruction;

wherein the instruction execution portion executes the decoded subsequent execution condition command instruction; and

wherein the instruction overriding control portion checks the execution result of the subsequent execution condition command instruction to determine whether the execution condition is satisfied, and overrides the subsequent instruction if the condition is not satisfied.

14. The data processing device according to Claim 13, wherein the conditional instruction and the subsequent instruction each include an instruction group including a plurality of instruction strings.

15. A program conversion device for reading in a descriptive program and converting it into a machine language program, the program conversion device comprising:

a first instruction detection portion for detecting from instruction strings of the descriptive program an instruction for which there is a possibility that a state of a processor is updated;

a second instruction detection portion for detecting from the entered instruction strings a conditional instruction that is executed depending on a state of the processor;

a first judgment portion for judging whether there is an instruction detected by the second instruction detection portion that follows an instruction detected by the first instruction detection portion;

a command instruction retrieval portion for retrieving from the machine language instruction code a subsequent execution condition command instruction, which indicates the same process execution as the instruction detected by the first instruction detection portion, and which indicates the execution condition of the subsequent conditional instruction;

an instruction rewriting portion for rewriting an instruction string detected by the first instruction detection portion and the second instruction detection portion into (a) a condition hiding instruction corresponding to the conditional instruction from which the condition has been eliminated and (b) the subsequent execution condition command instruction.

16. The program conversion device according to Claim 15, wherein the conditional instruction and the subsequent instruction each include an instruction group including a plurality of instruction strings.

17. A data processing device according to Claim 1, wherein the instruction overriding control portion lets the fetch portion skip the reading in of the subsequent instruction that is overridden.

18. A data processing device according to Claim 2, wherein the instruction overriding control portion lets the fetch portion skip the reading in of the subsequent instruction that is overridden.

19. A data processing device according to Claim 5, wherein the instruction overriding control portion lets the fetch portion skip the reading in of the subsequent instruction that is overridden.

20. A data processing device according to Claim 6, wherein the instruction overriding control portion lets the fetch portion skip the reading in of the subsequent instruction that is overridden.

21. A data processing device according to Claim 9, wherein the instruction overriding control portion lets the fetch portion skip the reading in of the subsequent instruction that is overridden.

22. A data processing device according to Claim 10, wherein the instruction overriding control portion lets the fetch portion skip the reading in of the subsequent instruction that is overridden.

23. A data processing device according to Claim 13, wherein the instruction overriding control portion lets the fetch portion skip the reading in of the subsequent instruction that is overridden.

24. A data processing device according to Claim 14, wherein the instruction overriding control portion lets the fetch portion skip the reading in of the subsequent instruction that is overridden.